



1/36

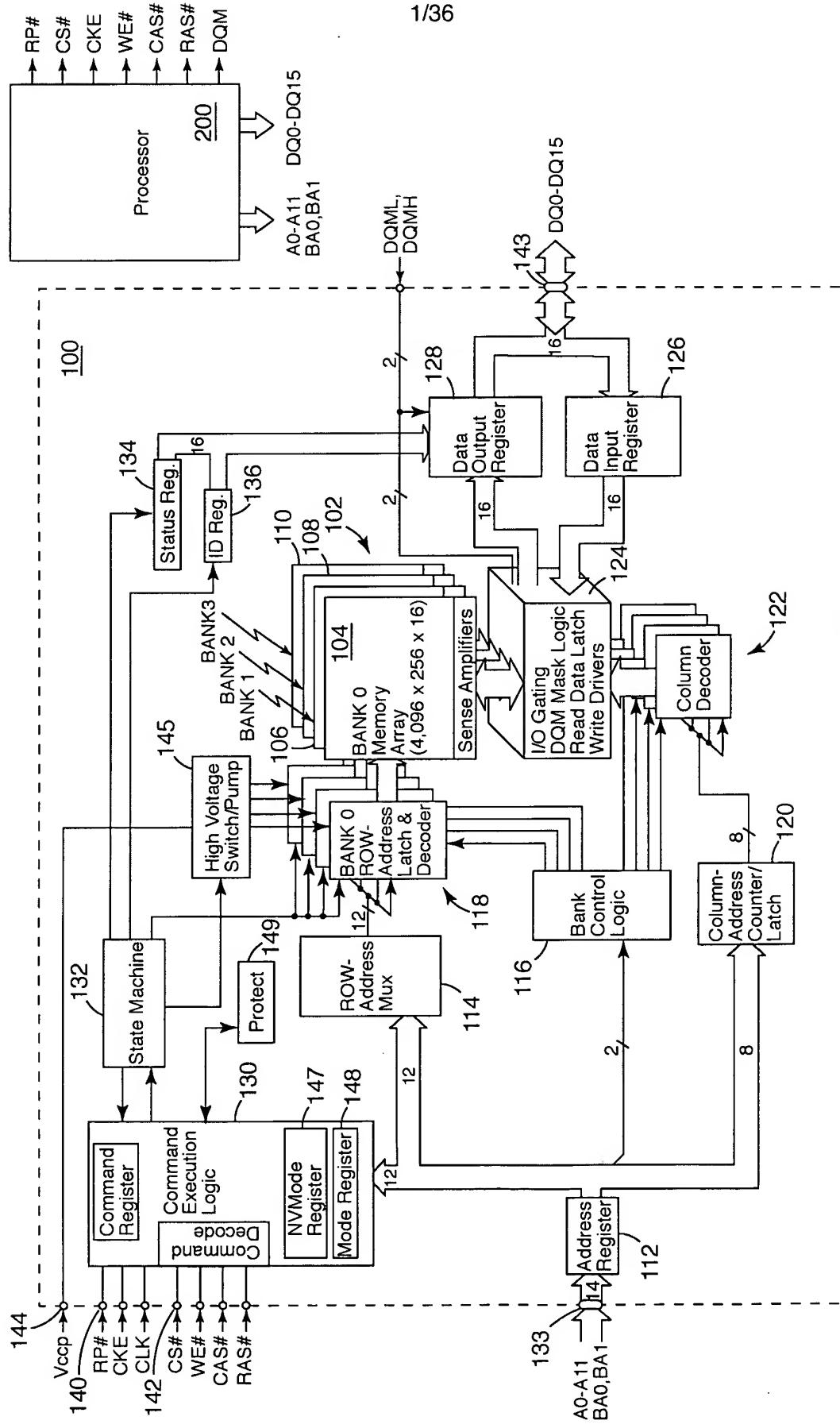


FIG. 1A

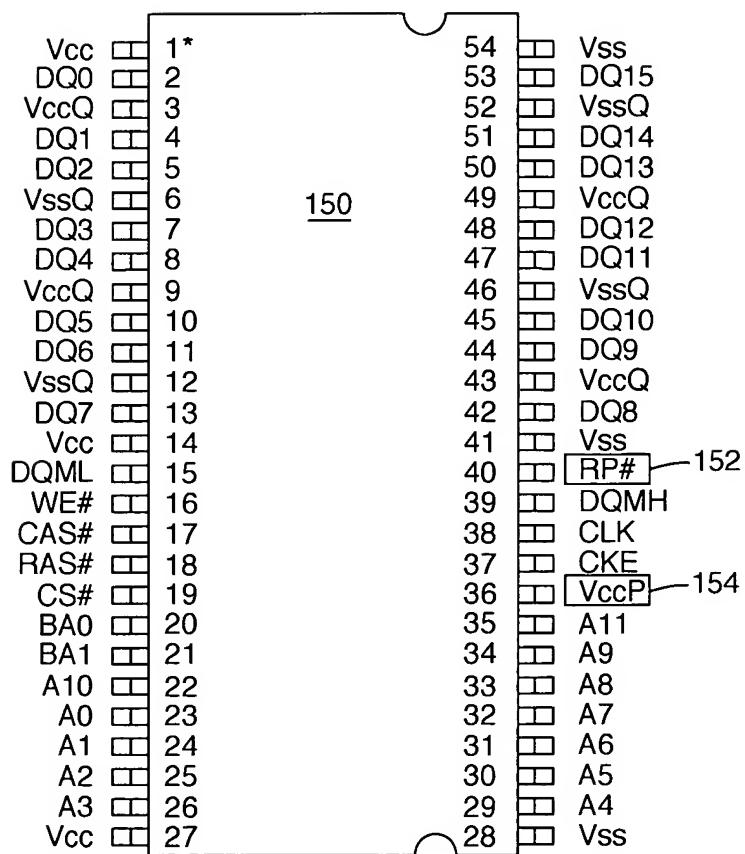


FIG. 1B

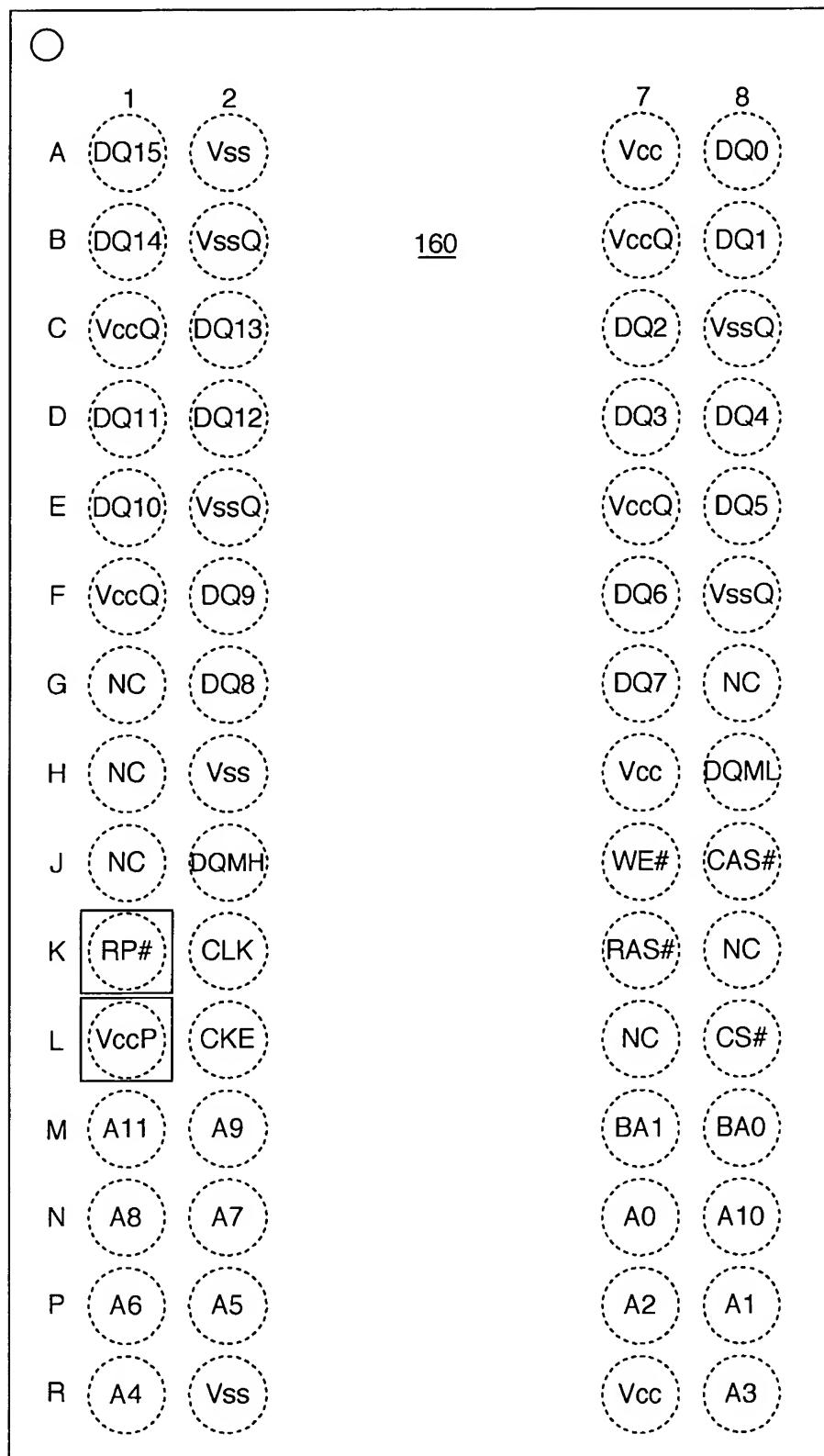


FIG. 1C

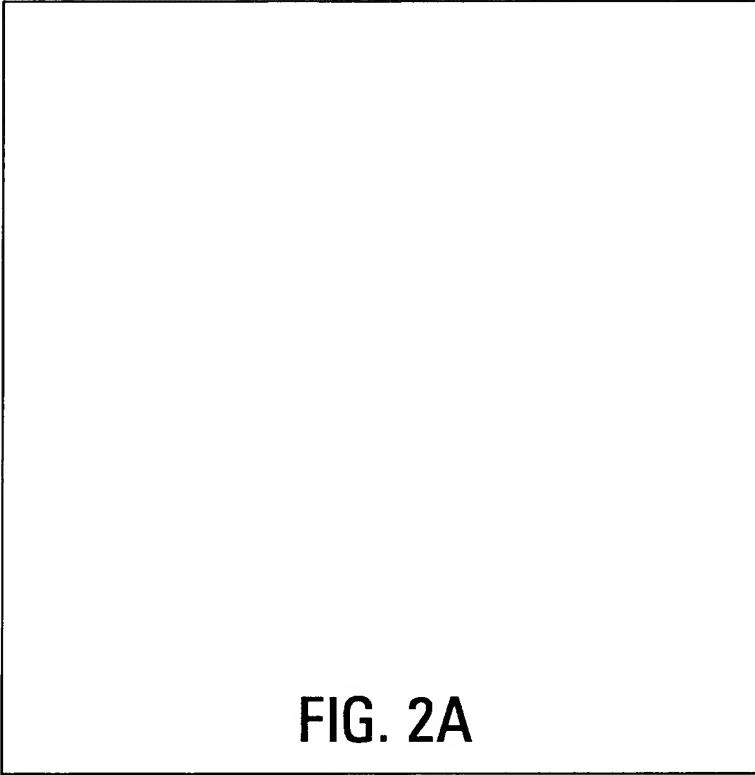


FIG. 2A

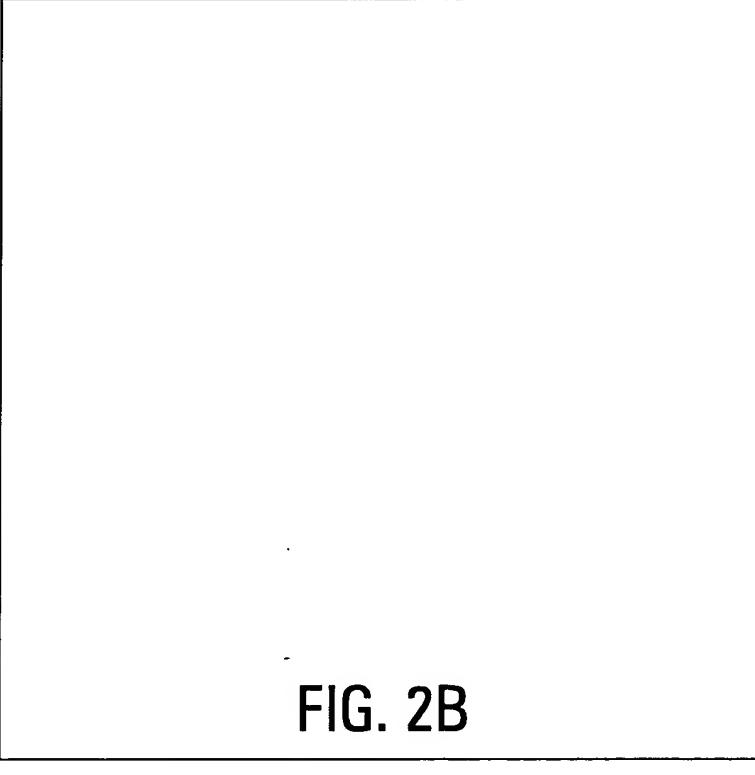


FIG. 2B

FIG. 2

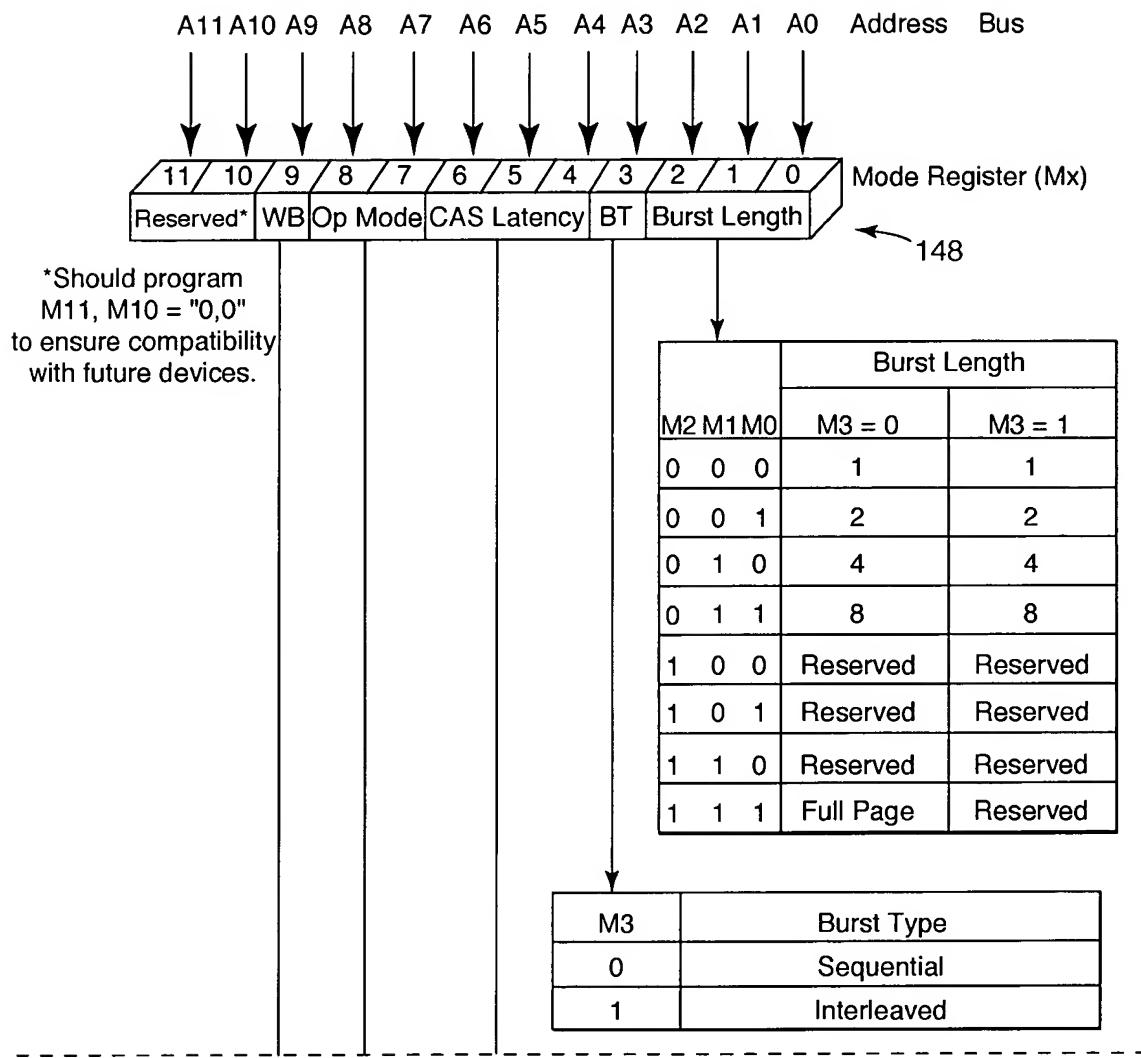


FIG. 2A

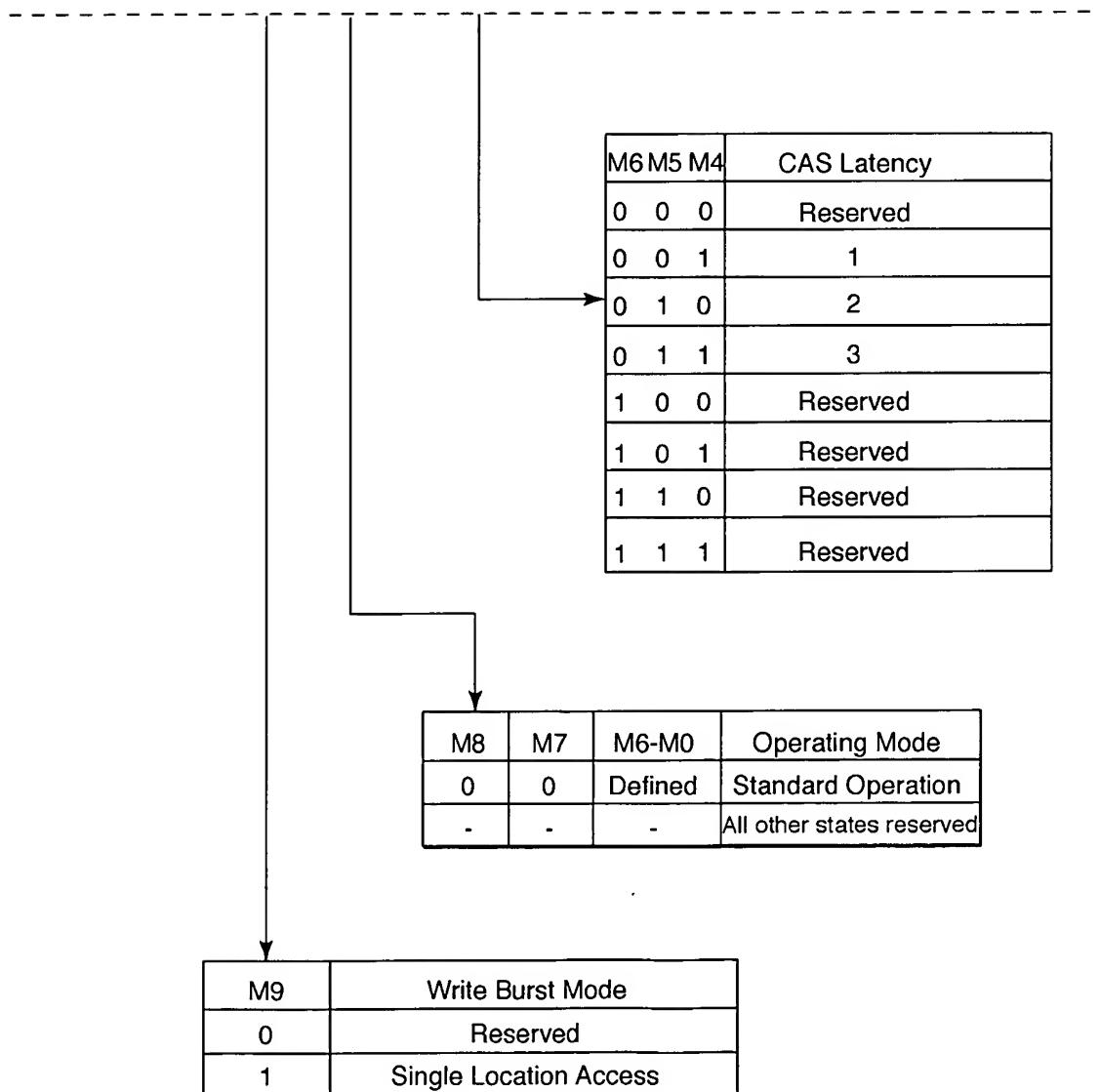


FIG. 2B

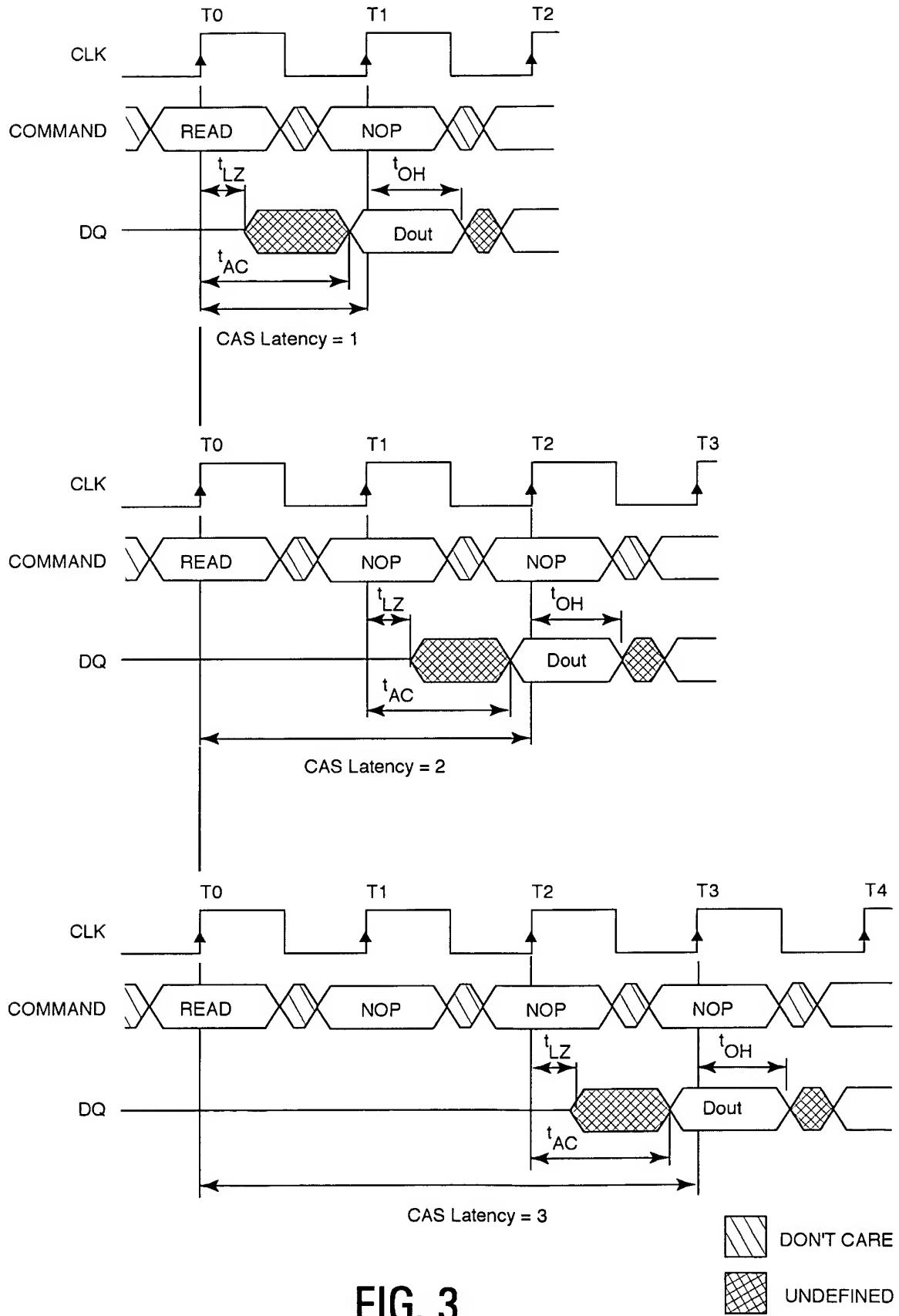
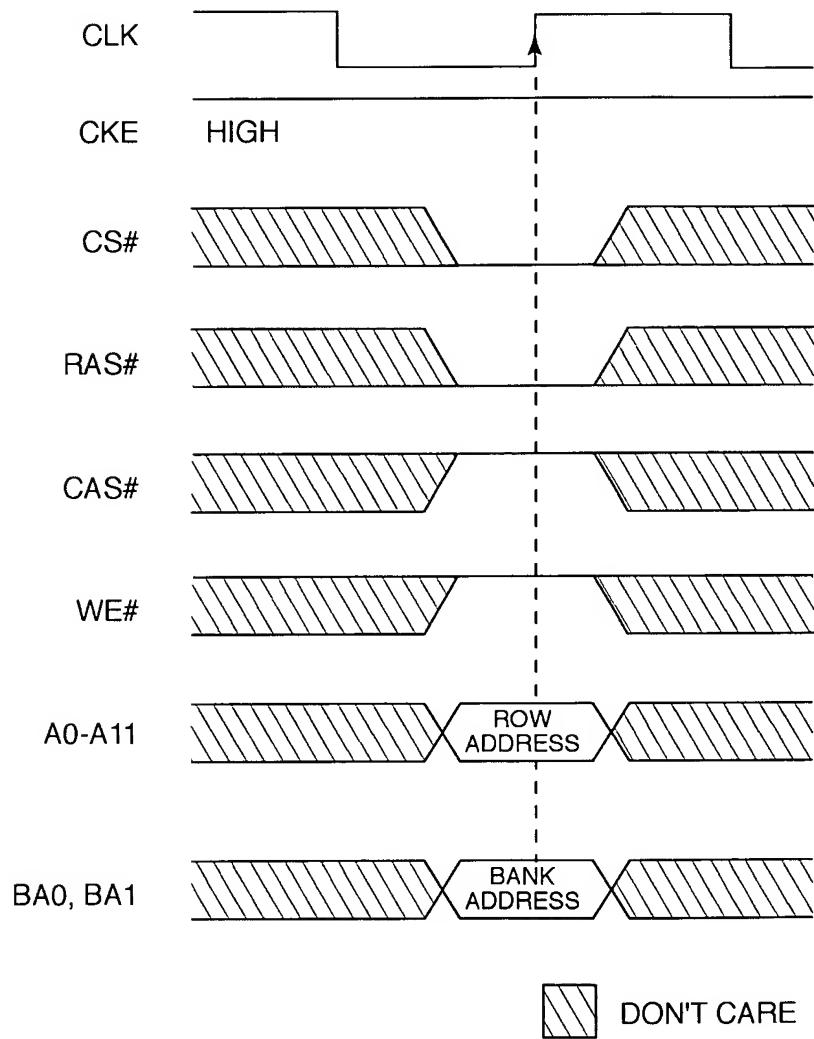


FIG. 3

**FIG. 4**

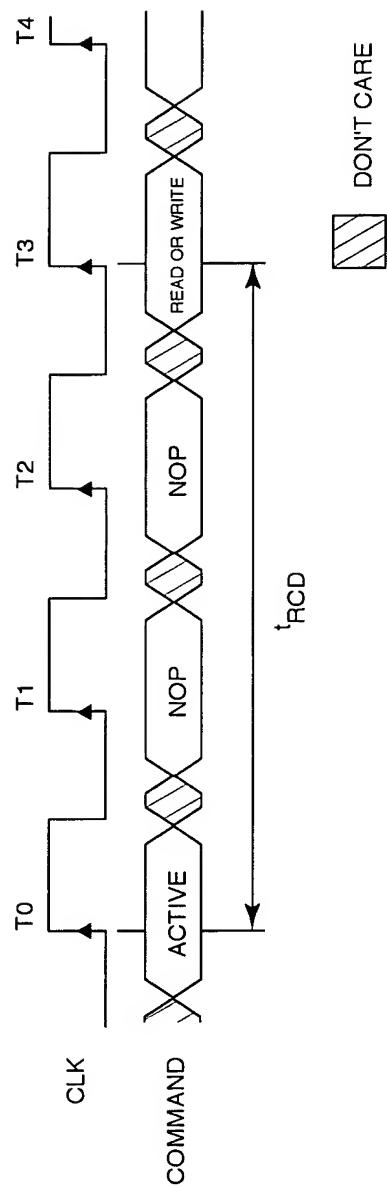


FIG. 5

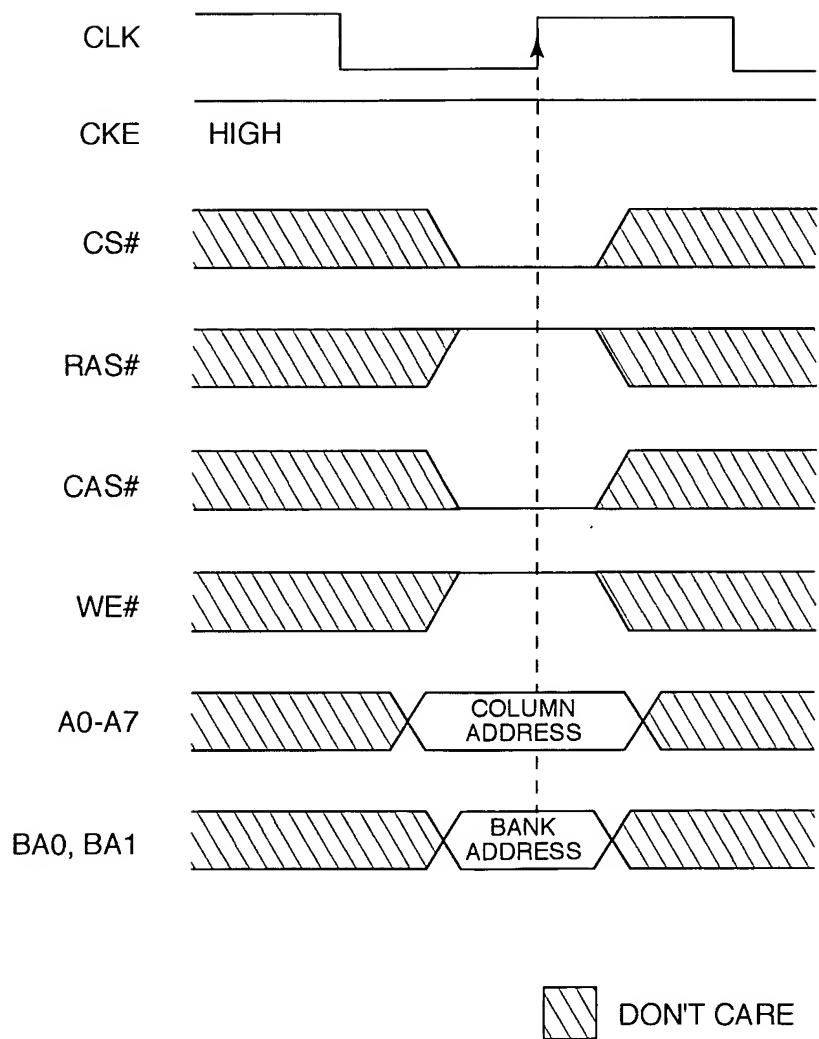
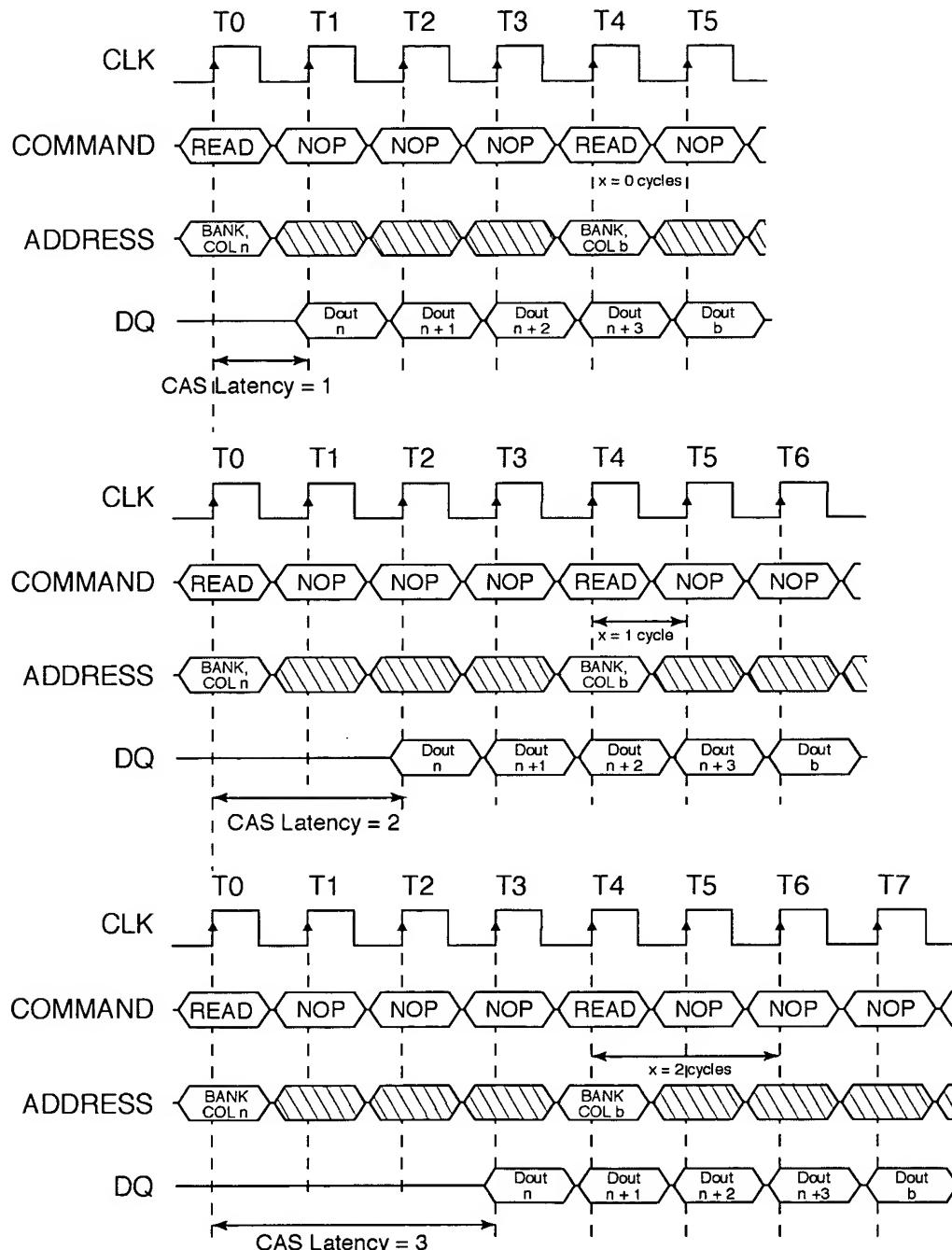
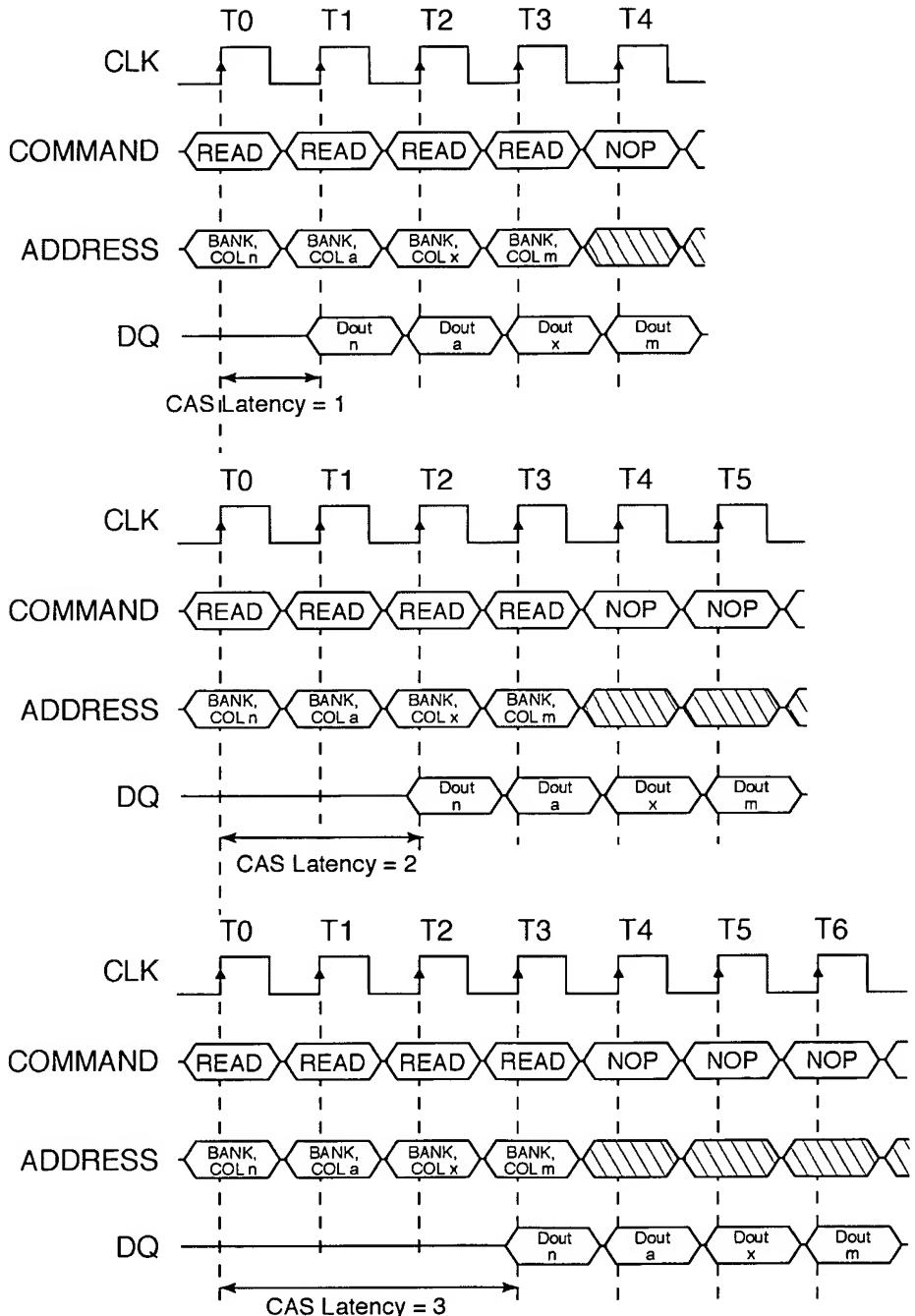


FIG. 6



NOTE: Each READ command may be to either bank. DQM is LOW.

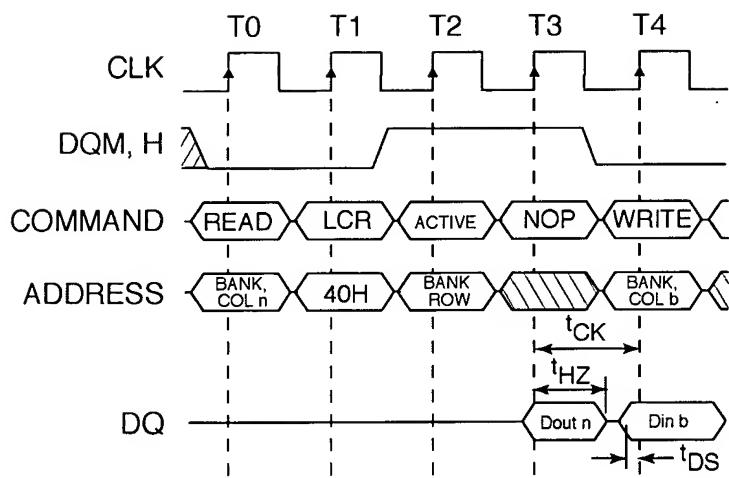
FIG. 7



DON'T CARE

NOTE: Each READ command may be to either bank. DQM is LOW.

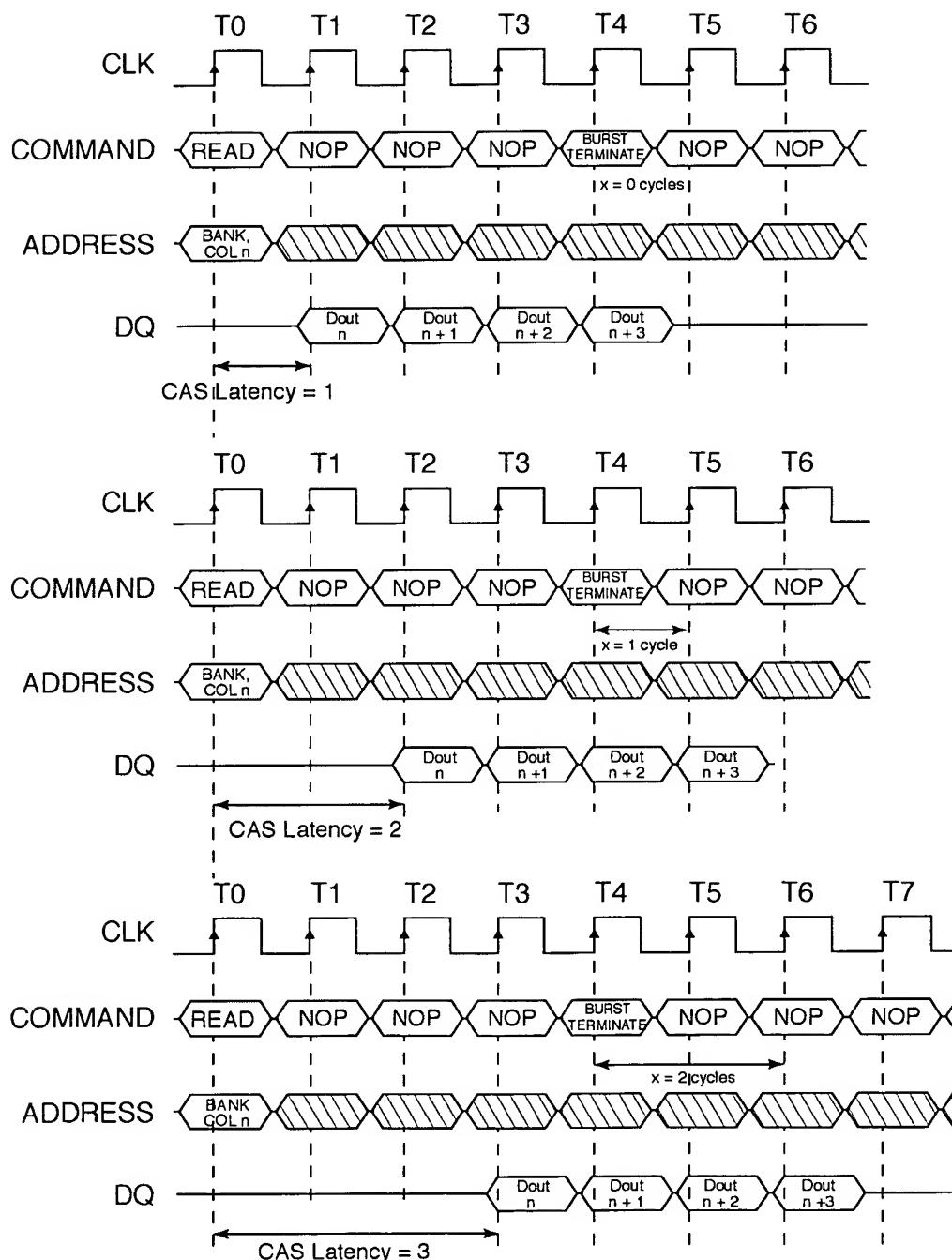
FIG. 8



NOTE: A CAS latency of three is used for illustration. The READ command may be to any bank, and the WRITE command may be to any bank. If a CAS latency of one is used, then DQM is not required.

DONT CARE

FIG. 9



NOTE: DQM is LOW.

FIG. 10

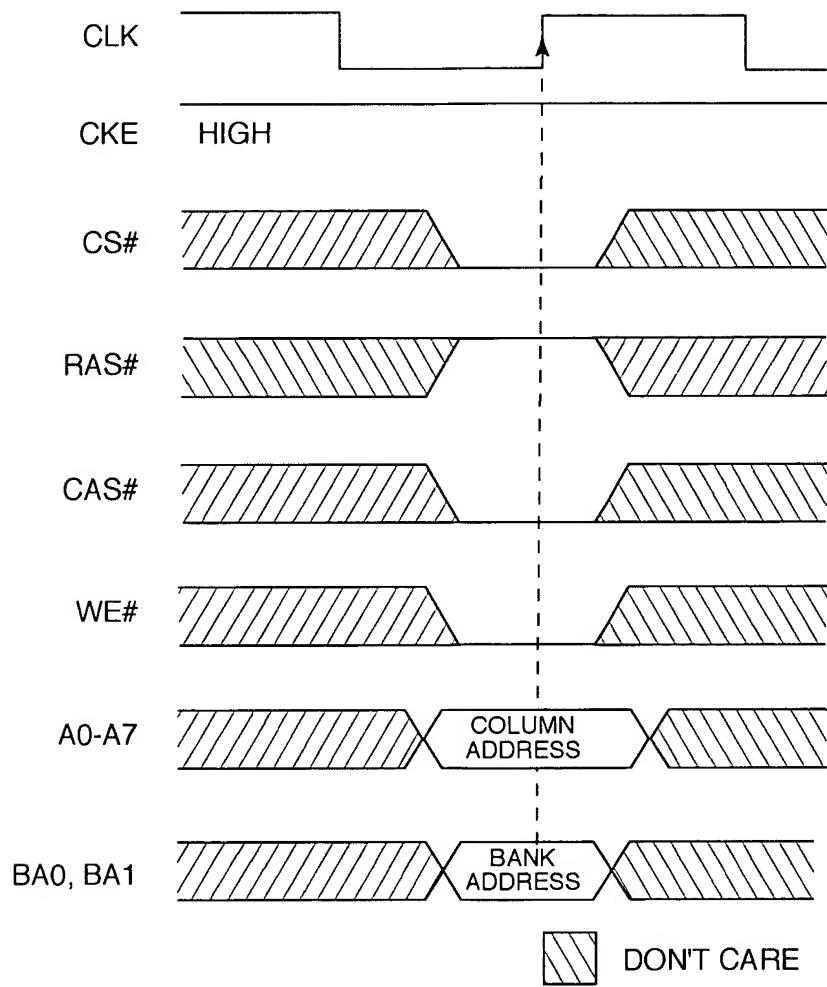
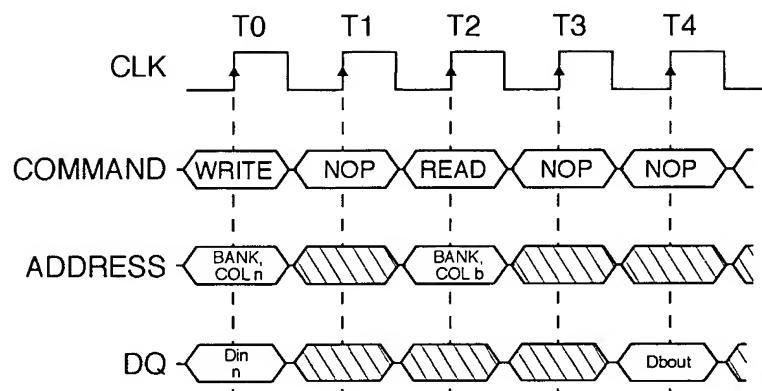


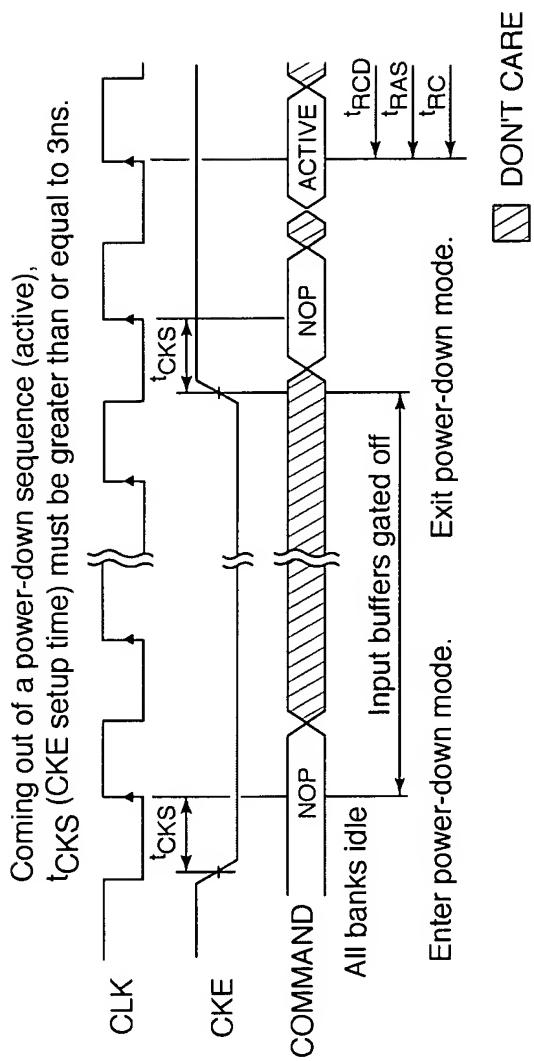
FIG. 11



NOTE: A CAS latency of two is used for illustration. The WRITE command may be to any bank and the READ command may be to any bank. DQM is LOW . A READ to the bank undergoing the WRITE ISM operation may output invalid data.

DON'T CARE

FIG. 12

**FIG. 13**

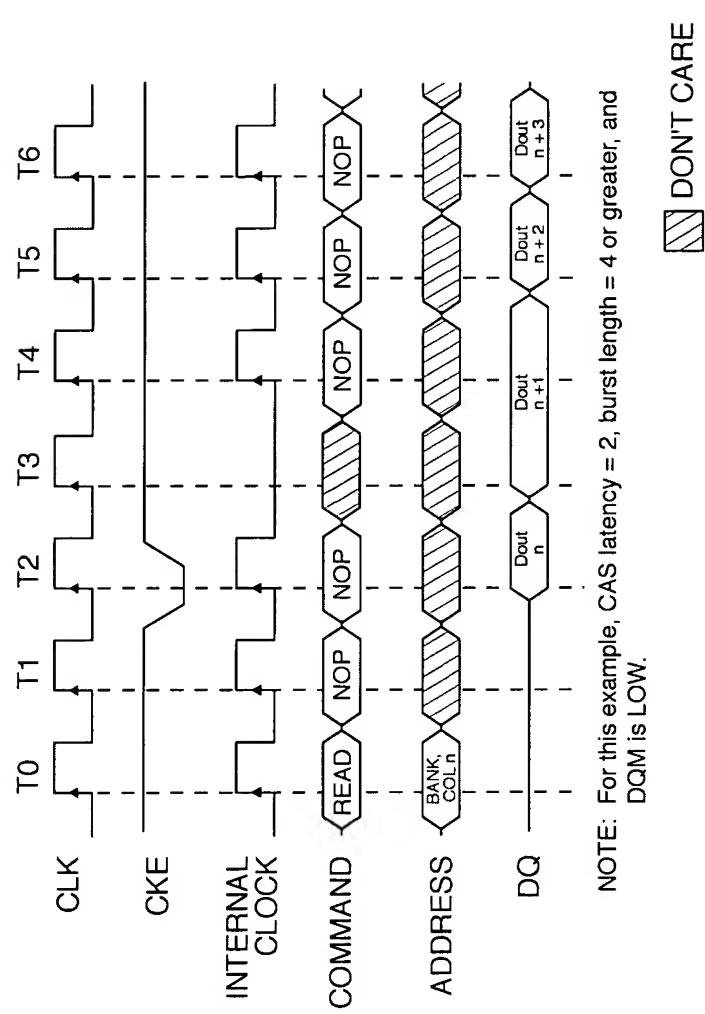


FIG. 14

ADDRESS RANGE

Bank			Row	Column	
Bank 3	Bank 2	Bank 1	Bank 0		
3	3	3	3	FFF	256K-Word Block 15
				C00	00H
				BFF	FFH
				800	00H
				7FF	FFH
				400	00H
				3FF	FFH
				000	00H
				FFF	FFH
				C00	00H
				BFF	FFH
				800	00H
				7FF	FFH
				400	00H
				3FF	FFH
				000	00H
				FFF	FFH
				C00	00H
				BFF	FFH
				800	00H
				7FF	FFH
				400	00H
				3FF	FFH
				000	00H
				FFF	FFH
				C00	00H
				BFF	FFH
				800	00H
				7FF	FFH
				400	00H
				3FF	FFH
				000	00H
				FFF	FFH
				C00	00H
				BFF	FFH
				800	00H
				7FF	FFH
				400	00H
				3FF	FFH
				000	00H

Word-wide (x16)

 Software Lock = Hardware-Lock Sectors

RP# = V_{HH} to unprotect if either the block protect or device protect bit is set.

 Software Lock = Hardware-Lock Sectors

RP# = V_{CC} to unprotect but must be V_{HH} if the device protect bit is set.

See BLOCK PROTECT/UNPROTECT SEQUENCE for detailed information.

FIG. 15

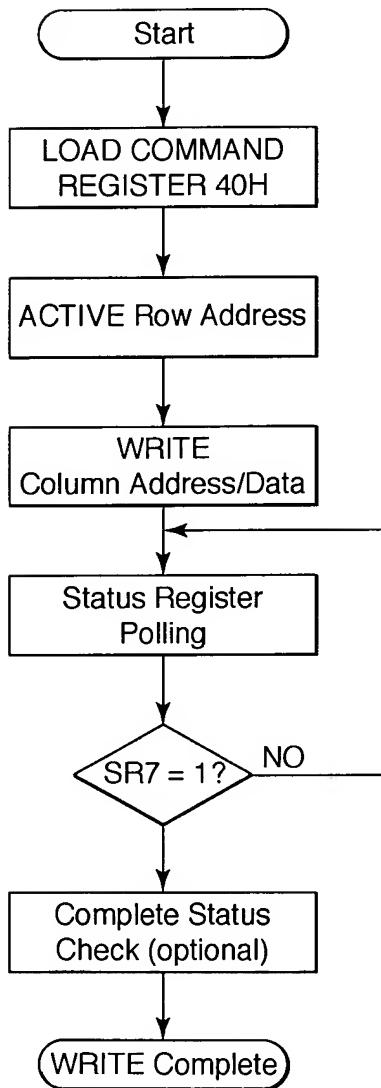


FIG. 16

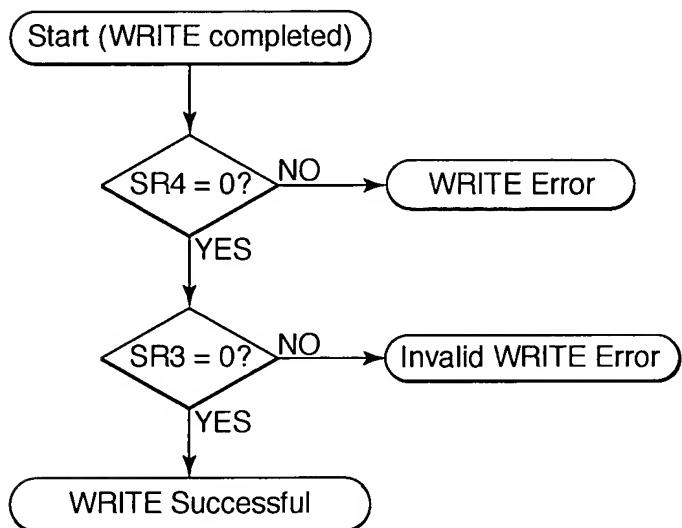


FIG. 17

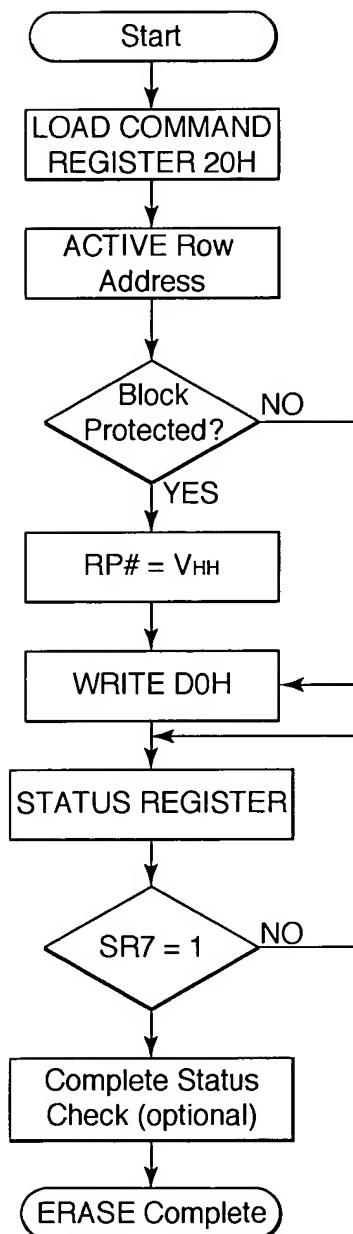


FIG. 18

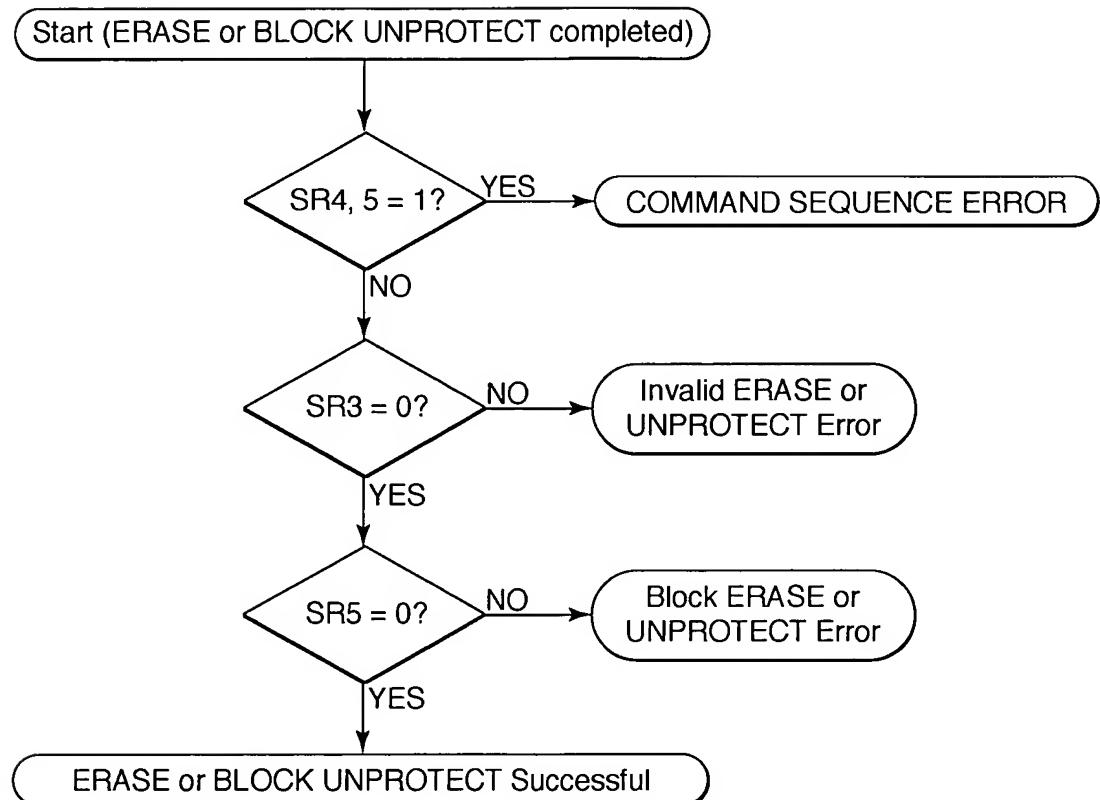


FIG. 19

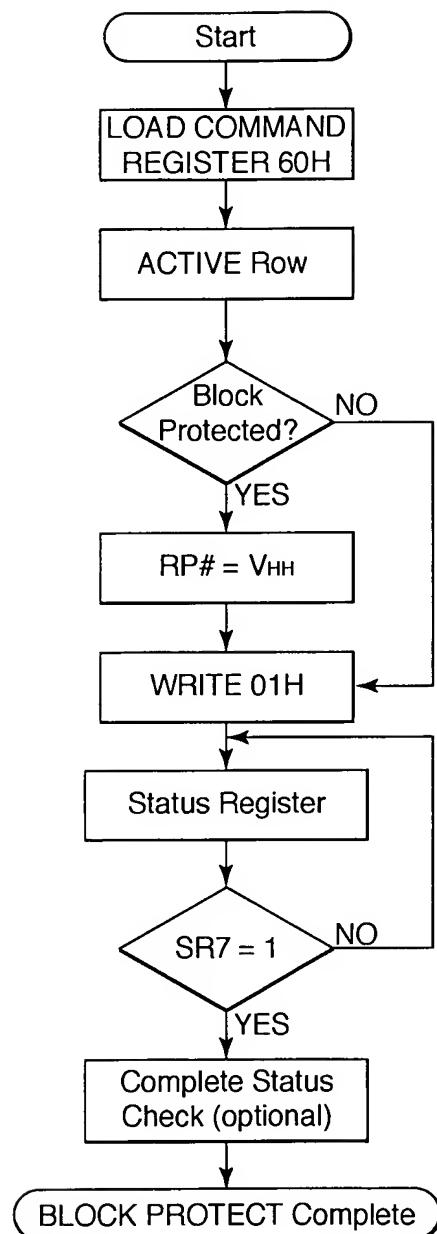


FIG. 20

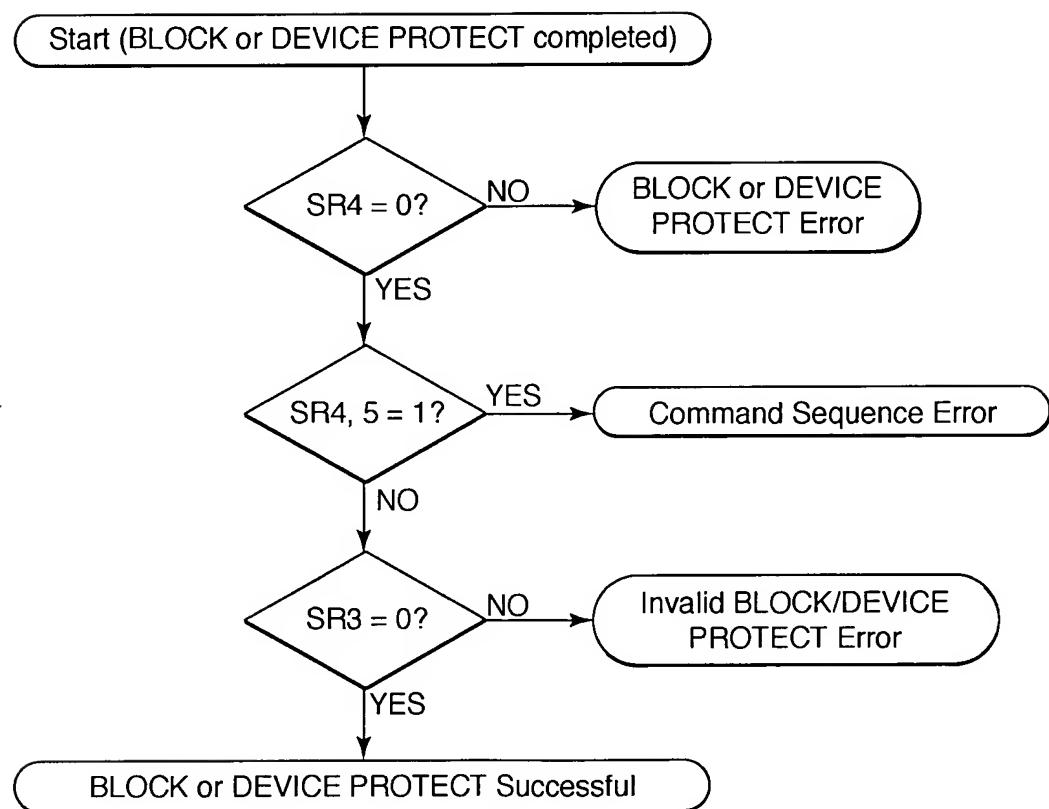


FIG. 21

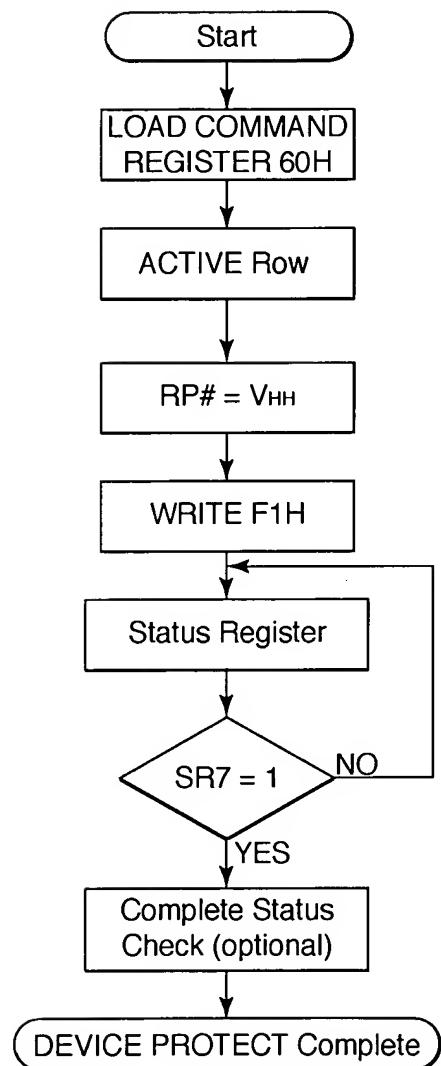


FIG. 22

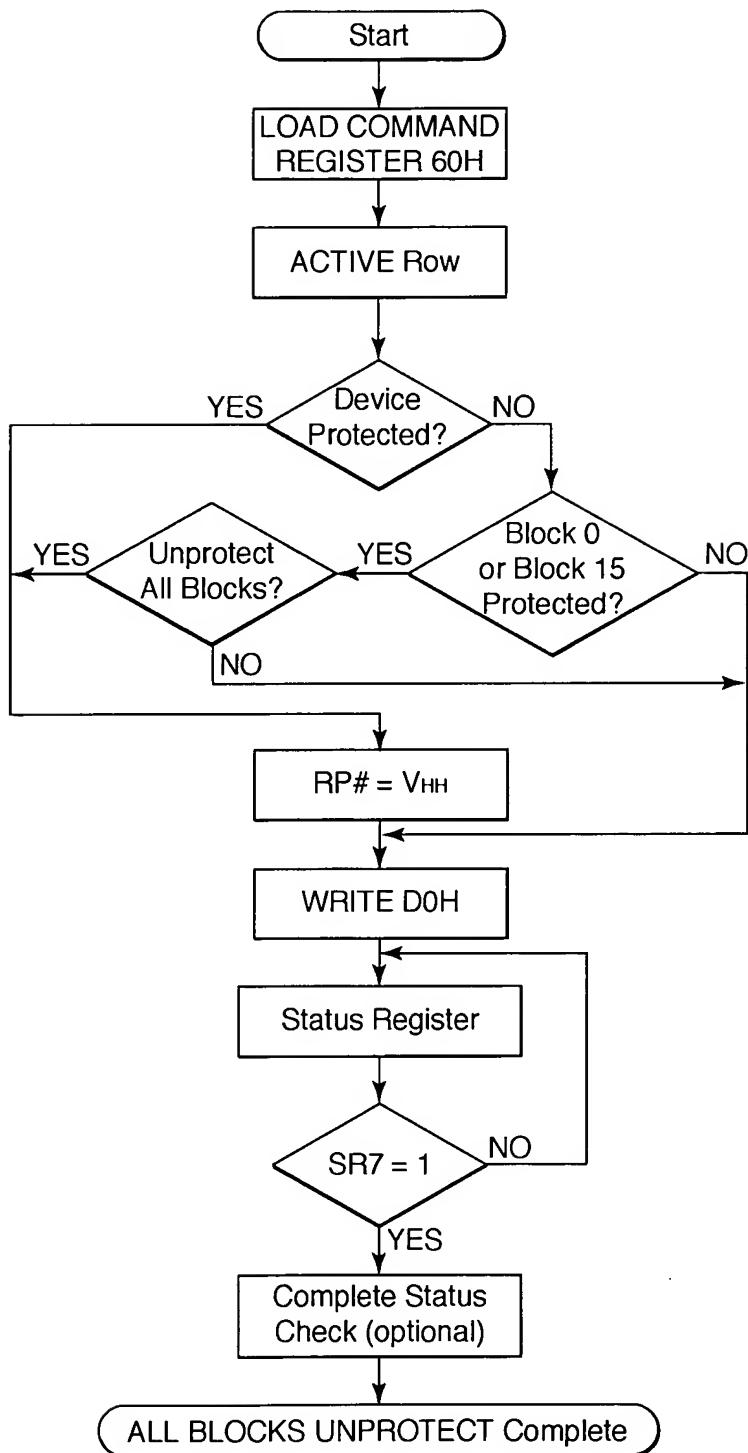


FIG. 23

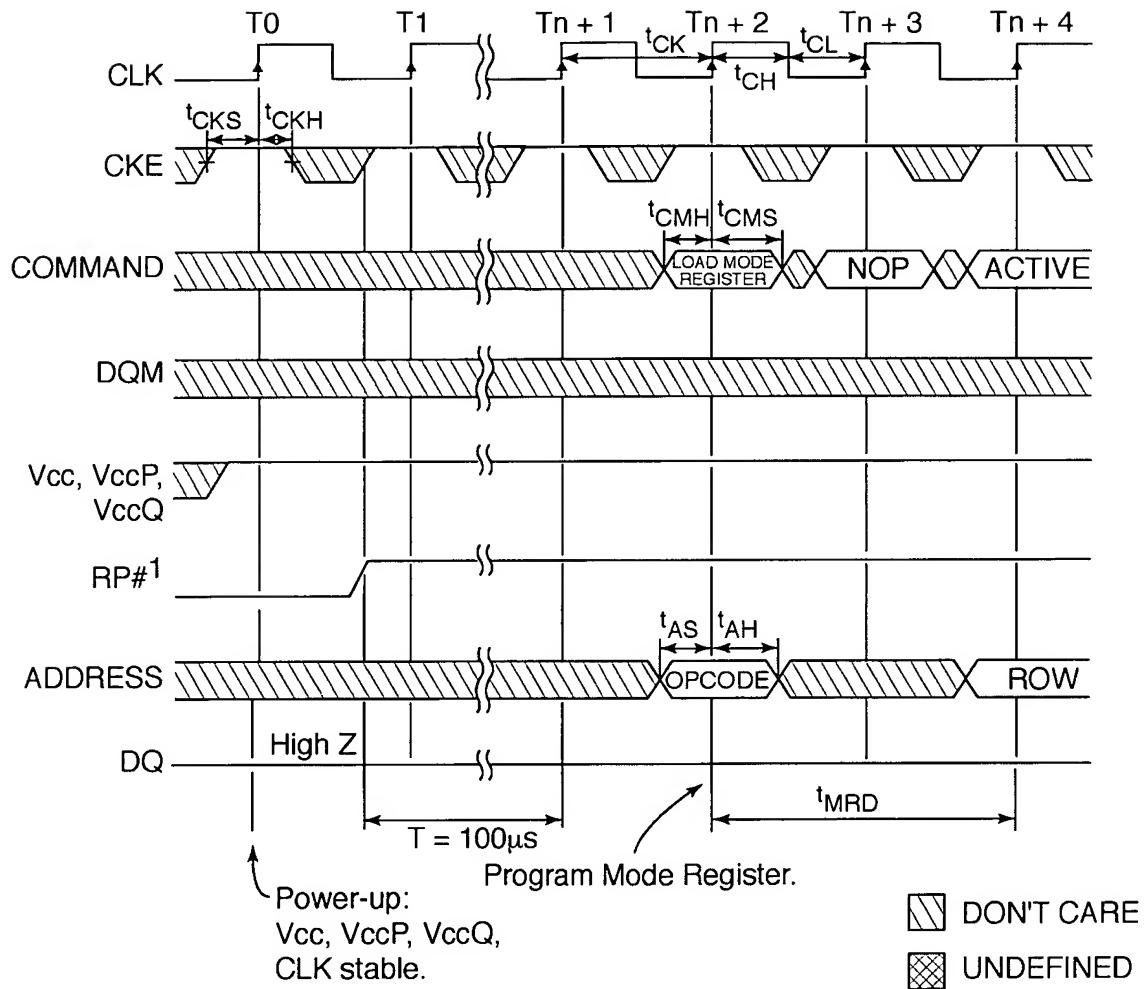


FIG. 24

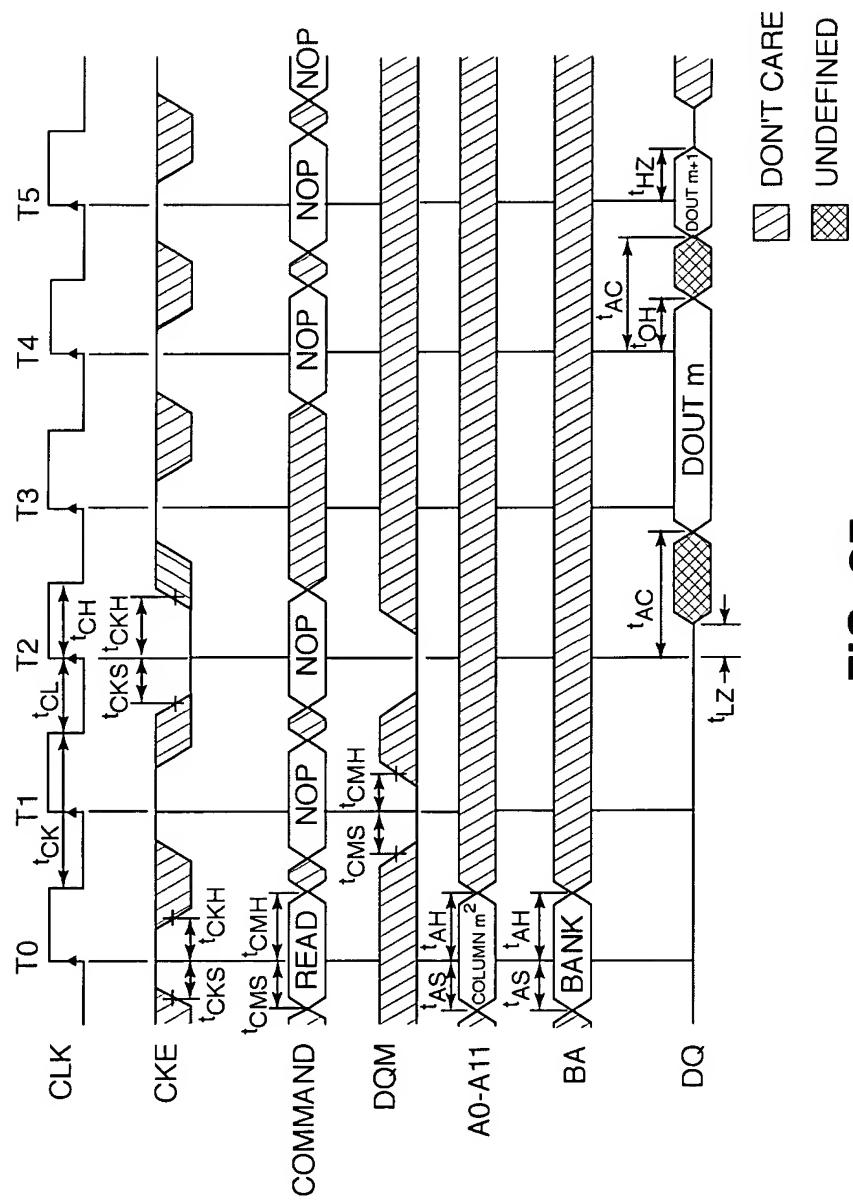


FIG. 25

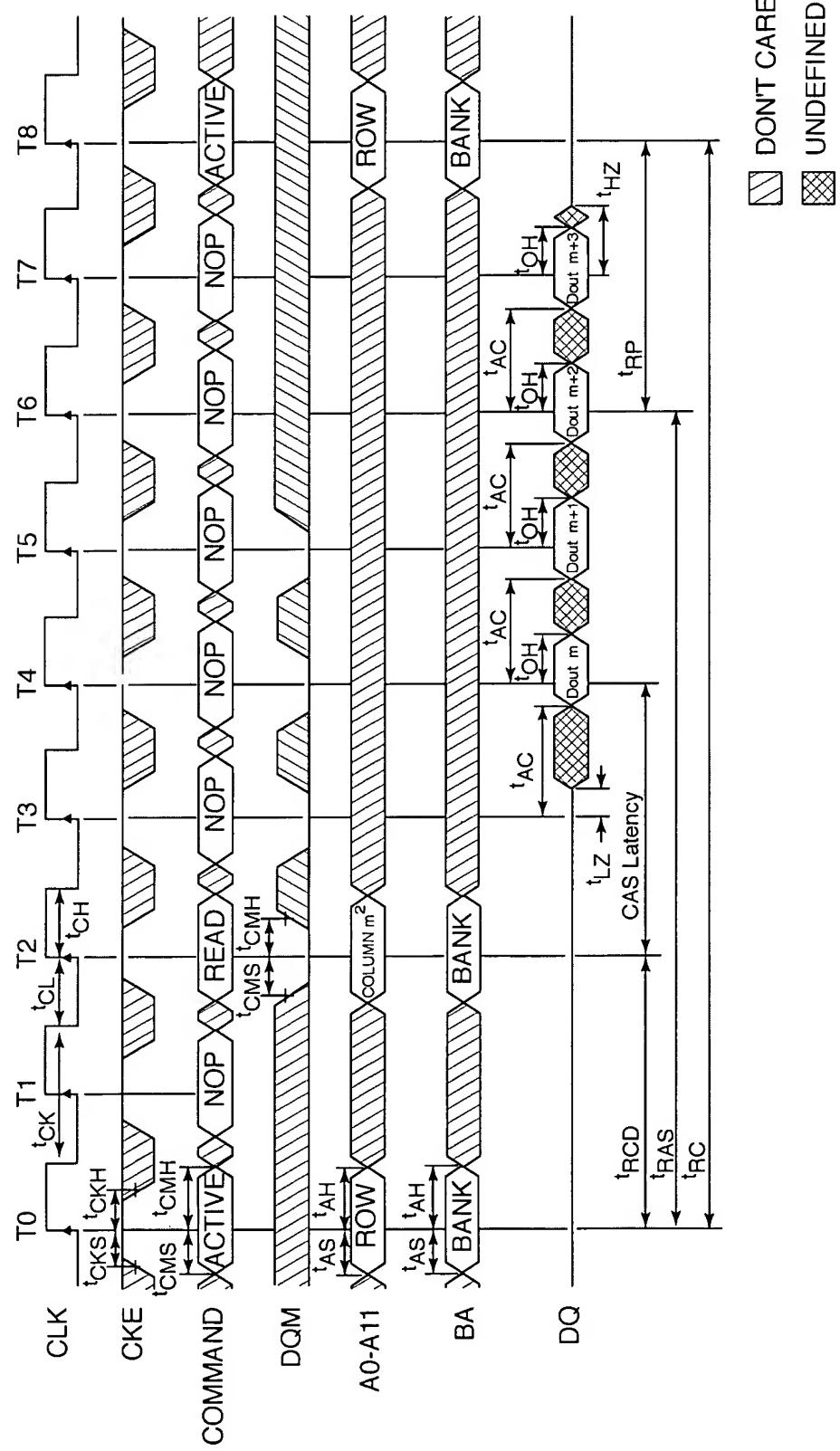


FIG. 26

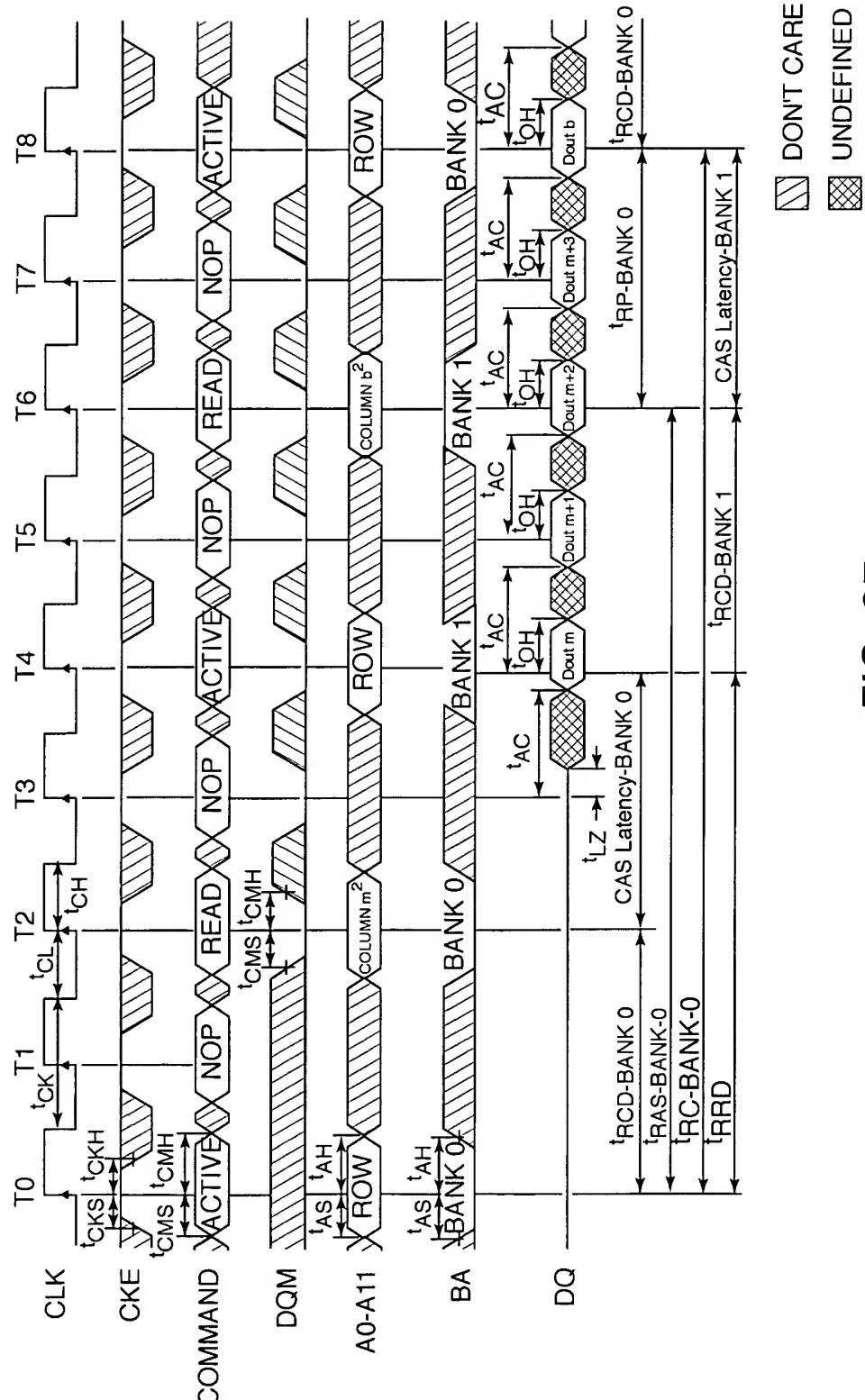


FIG. 27

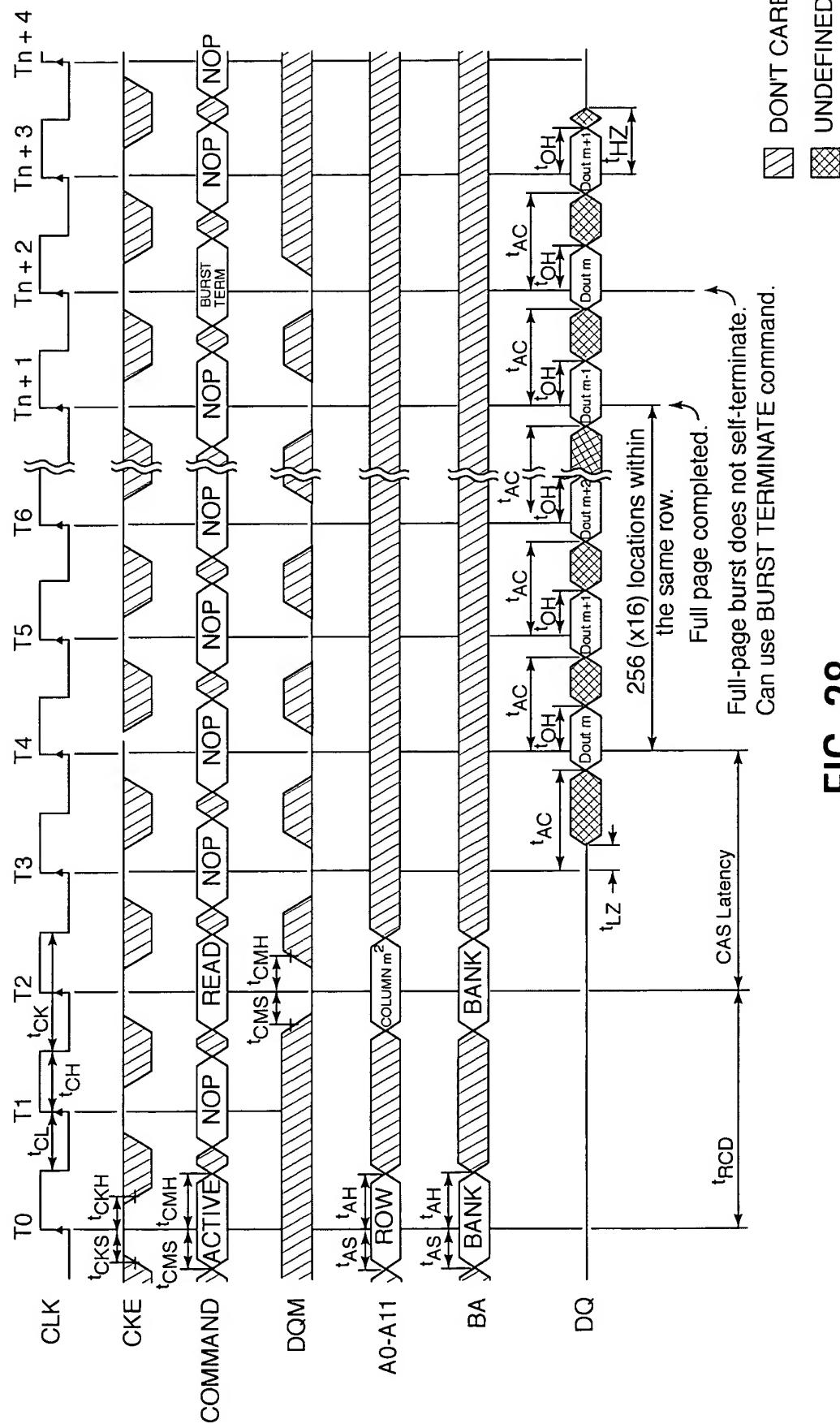


FIG. 28

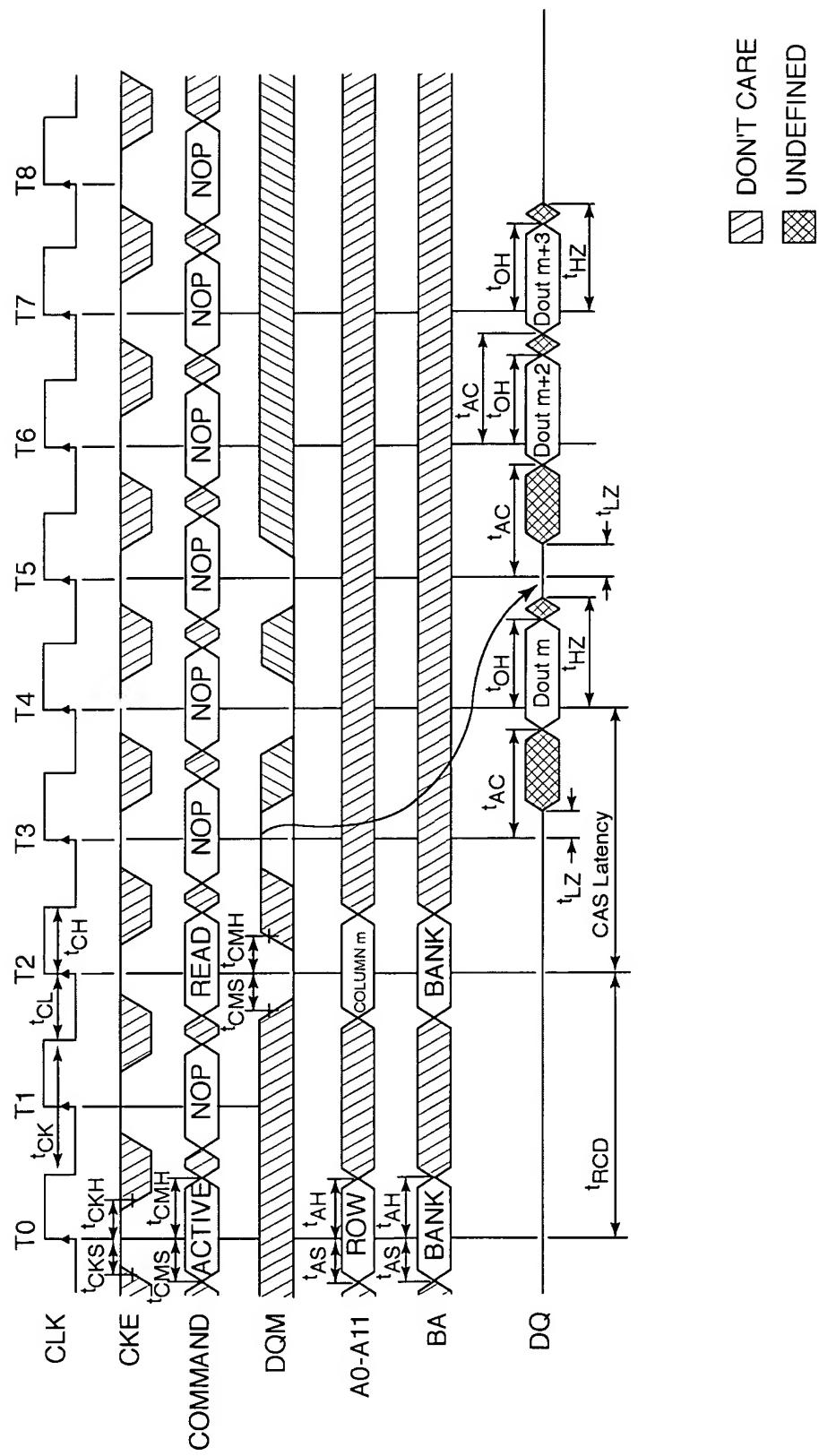


FIG. 29

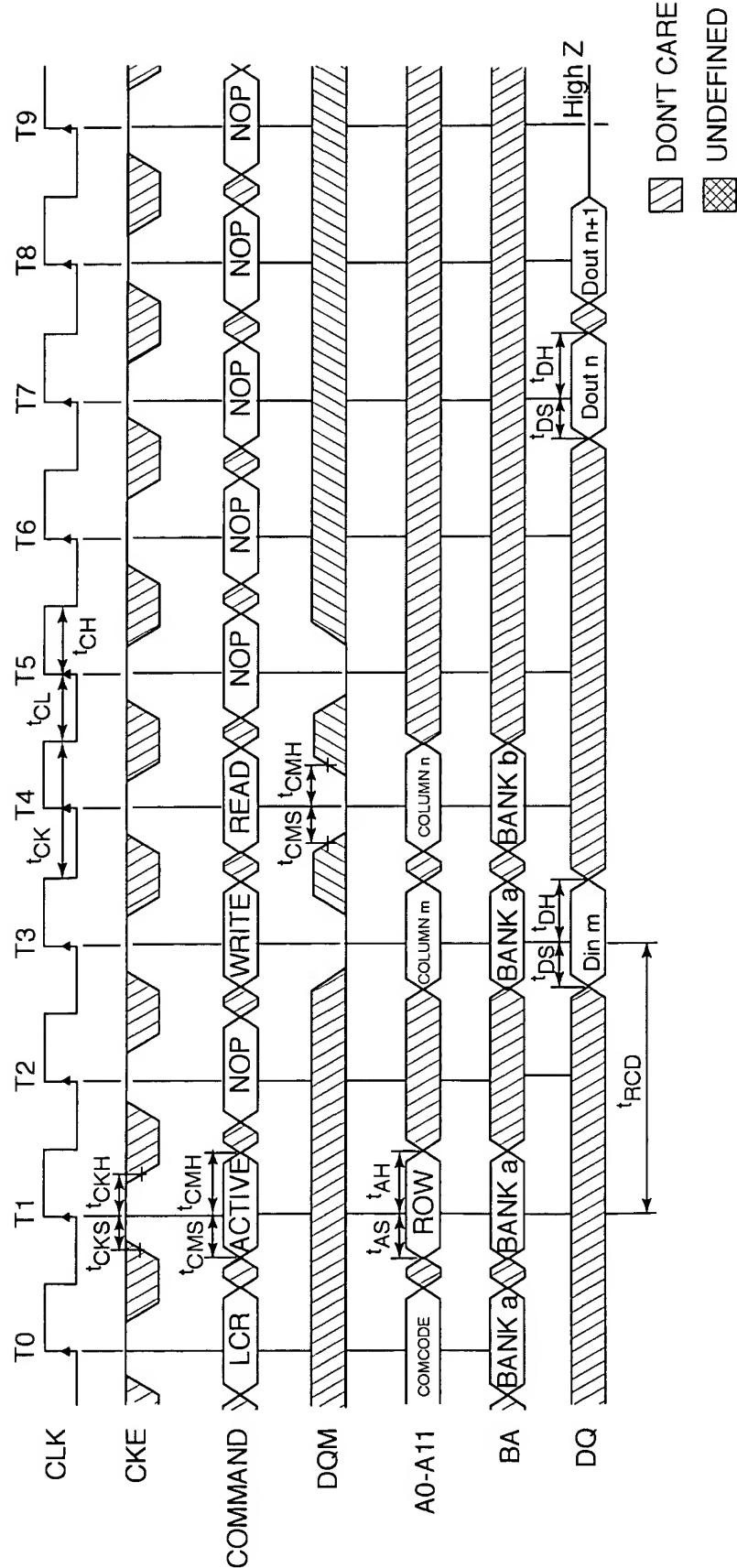


FIG. 30

35/36

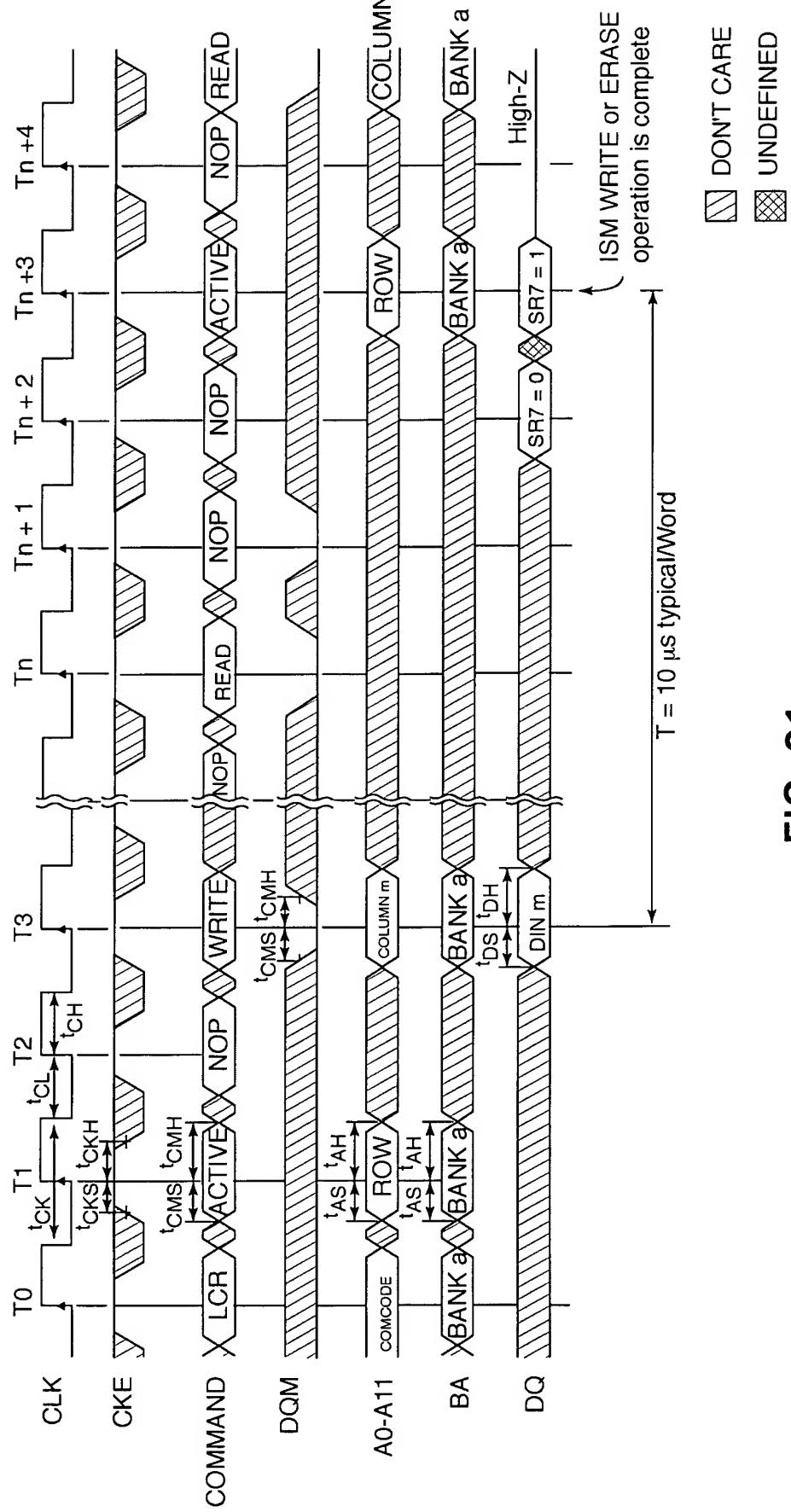


FIG. 31

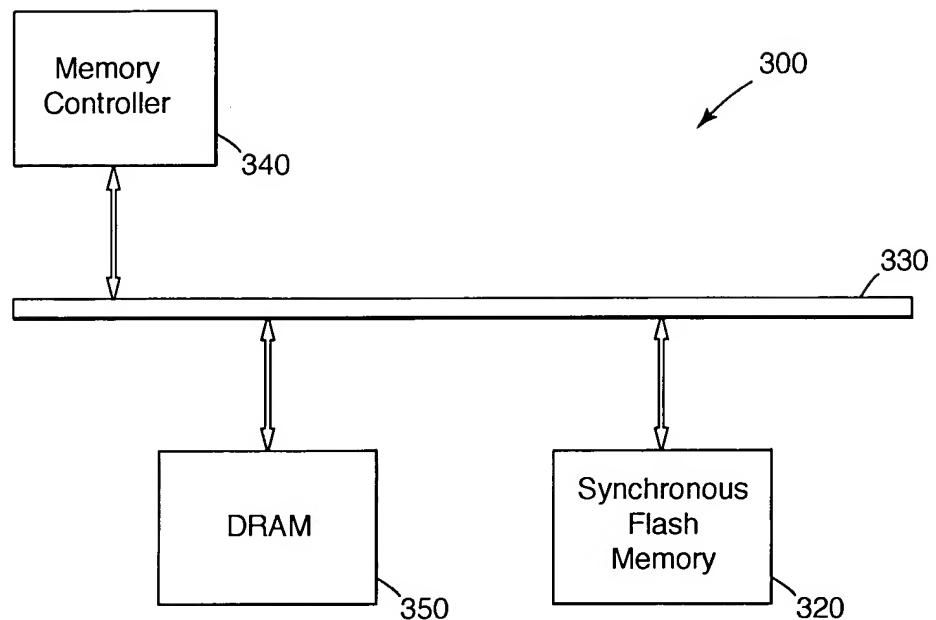


FIG. 32